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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,670	09/12/2003	Josephus A.E.P. van Engelen	1875.4690000	7574
26111 7590 06/22/2007 STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER ZAMAN, FAISAL M	
			ART UNIT 2111	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/660,670

Applicant(s)

VAN ENGELEN ET AL.

Examiner

Faisal Zaman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 02 May 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-16 and 18-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 and 18-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Response to Amendment***

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **Claims 1, 2, and 18-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson (U.S. Patent No. 5,264,958), in view of Applicant's Admitted Prior Art (hereinafter "AAPA").

**Regarding Claims 1 and 18**, Johnson discloses a serial data interface system (Johnson, Figure 1, item 18 and Figure 3, Column 3, lines 57-68) comprising:

A first transceiver (Johnson, Figure 3, item 28 with item 33, Column 4 line 67 – Column 5 line 34) configured to comply with a first standard (Johnson, Column 5, lines 18-22; ie. the V.35 standard) coupled to a set of pins of an interface (Johnson, Figure 3, item 20, Column 4, lines 33-37); and

A second transceiver (Johnson, Figure 3, item 28 with item 35, Column 4 line 67 – Column 5 line 34) configured to comply with a second standard (Johnson, Column 5, lines 18-22; ie. the X.21 standard) coupled to the set of pins, wherein the interface can transmit and receive a signal and can electronically change between the first and second standard depending on the signal being transmitted or received (Johnson, Column 4, lines 43-46 and lines 54-59; ie. communications processor 22 receives cable

identification bits 27, and according to this identification electronically switches between the line drivers 33 and 35; further, in order to transmit a X.21 signal from communication processor 22 over cable 16, for example, line driver 35 must be used in order for proper data transmission).

Johnson does not expressly disclose wherein said first standard is a data-strobe standard; and

Wherein said second standard is a serializer-deserializer standard.

In the same field of endeavor (e.g. bilingual modes within a single port), AAPA teaches the common use of the IEEE 1394-1995/1394a-2000 (a data-strobe standard, as evidenced by AAPA, Page 1, paragraph 0002) and IEEE 1394b-2002 standards (a Beta and serializer-deserializer standard, as evidenced by AAPA, Page 6, Paragraph 0028) (AAPA, Page 1, Paragraph 0002).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined AAPA's teachings of bilingual modes within a single port with the teachings of Johnson, for the purpose of increasing compatibility among devices that comply with the IEEE 1394-1995/1394a-2000 and IEEE 1394b-2002 standards, which are well known to have much faster data transfer rates than the standards used in Johnson.

**Regarding Claims 2 and 20**, Johnson does not expressly disclose wherein the first standard is IEEE 1394-1995/1394a-2000 standard; and the second standard is IEEE 1394b-2002 standard.

In the same field of endeavor, AAPA teaches the common use of the IEEE 1394-1995/1394a-2000 and IEEE 1394b-2002 standards (AAPA, Page 1, Paragraph 0002).

The motivation that was used in the combination of Claim 1, super, applies equally as well to Claim 2.

**Regarding Claim 19**, Johnson teaches wherein steps (b) and (c) are performed substantially simultaneously (Johnson, Column 4, lines 54-59).

3. **Claims 3-16 and 21-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson in view of AAPA as applied to Claim 1 above (hereinafter "Johnson-AAPA"), and further in view of Oprescu et al. ("Oprescu") (U.S. Patent No. 5,559,967).

Johnson-AAPA discloses the system of Claim 1 as described above.

**Regarding Claim 3**, Johnson-AAPA does not expressly disclose wherein the first transceiver device comprises: a twisted-wire pair (TP) bias section; a first TP transceiver section; and a second TP transceiver section.

In the same field of endeavor (e.g. a dynamic, multi-speed bus architecture for enabling multi-speed data transfers on a bus having variable speed and fixed speed nodes connected thereto) Oprescu teaches wherein a first transceiver device (Oprescu, see figure 19, transceiver 14 and column 17 lines 2-12) comprises: a twisted-wire pair (TP) bias section; a first TP transceiver section; and a second TP transceiver section (Oprescu, see figure 19 and column 4 lines 7-11).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Oprescu's teachings of a dynamic, multi-speed bus architecture for enabling multi-speed data transfers on a bus having variable speed and fixed speed nodes connected thereto with the teachings of Johnson, for the purpose of providing a method and apparatus for the transfer of speed messages on a multi-speed bus independent of the data signal transfers (see Oprescu, Column 2, lines 16-19). Johnson-AAPA also provides motivation to combine by stating it is an object of the invention to provide a more efficient interface subsystem for use with a business machine for use in a communication or data network which is able to interface with one of a plurality of electrical interface standards (see Johnson, Column 2, lines 33-38).

**Regarding Claim 4**, Oprescu teaches the following limitation, which Johnson-AAPA does not expressly disclose: wherein the TP bias section comprises: a TP bias device; and a connection detection device (Oprescu, see figure 4 and column 3 lines 29-31).

The motivation utilized in the combination of Claim 3, *super*, applies equally as well to Claim 4.

**Regarding Claims 5-8**, Oprescu teaches the following limitation, which Johnson-AAPA does not expressly disclose: wherein the first TP-transceiver section comprises:

A strobe signal device; a data signal device; an arbitration signal device; and a speed detection device (Oprescu, see figure 3A).

The motivation utilized in the combination of Claim 3, super, applies equally as well to Claims 5-8.

**Regarding Claims 9-14**, Oprescu teaches the following limitation, which Johnson-AAPA does not expressly disclose: wherein the second transceiver comprises: a transmitter section coupled to the second pin; and a receiver section coupled to the first pin (Oprescu, see figures 3A-3B, 4, 13, 19).

The motivation utilized in the combination of Claim 3, super, applies equally as well to Claims 9-14.

**Regarding Claim 15**, Johnson-AAPA discloses a serial data interface system (Johnson, Figure 1, item 18 and Figure 3, Column 3, lines 57-68), comprising a single port (Johnson, Figure 3, item 20) comprising:

A first section (Johnson, Figure 3, item 28 with item 33, Column 4 line 67 – Column 5 line 34) configured to comply with a first standard wherein the first standard is a data-strobe standard (AAPA, Page 1, paragraph 0002, ie. IEEE 1394-1995/1394a-2000 [a data-strobe standard]); and

A second section (Johnson, Figure 3, item 28 with item 35, Column 4 line 67 – Column 5 line 34) configured to comply with a second standard wherein said second standard is a serializer-deserializer standard (AAPA, Page 1, paragraph 0002; ie. IEEE

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1394b-2002 standard, which is a Beta and serializer-deserializer standard, as evidenced by AAPA, Page 6, Paragraph 0028).

Johnson-AAPA does not expressly disclose wherein the first section includes, a TPBIAS device section coupled to first and second pins (through additional circuitry), a first transceiver section coupled to the first and second pins, and a second transceiver section coupled to third and fourth pins, and the second section configured to comply with a second standard including, a signal transmitting device coupled to the third and fourth pins, and a signal receiving device coupled to the first and second pins.

In the same field of endeavor, Oprescu teaches a first section (Oprescu, first node 21) configured to comply with a first mode including, a TPBIAS device section coupled to first and second pins (through additional circuitry), a first transceiver section coupled to the first and second pins (Oprescu, see figure 19, transceiver 14, signals 40, 41), and a second transceiver section coupled to third and fourth pins (Oprescu, see figure 19, transceiver 18, signals 42, 43), and a second section (Oprescu, second node 23) configured to comply with a second mode including, a signal transmitting device coupled to the third and fourth pins, and a signal receiving device coupled to the first and second pins (Oprescu, see figure 19, node 23 coupling to signals 41-43).

The motivation utilized in the combination of Claim 3, super, applies equally as well to Claim 15.



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**Regarding Claim 16**, Johnson-AAPA teaches wherein the first standard is IEEE 1394-1995/1394a-2000 and the second standard is IEEE 1394b-2002 standard (AAPA, Paragraph 0002).

**Regarding Claims 21-24**, Oprescu teaches the following limitation, which Johnson-AAPA does not expressly disclose: wherein the first transceiver comprises: a bias section; a first transceiver section; and a second transceiver section (Oprescu, see figures 3A, 9).

The motivation utilized in the combination of Claim 3, super, applies equally as well to Claim 21-24.

#### ***Prior Art of Record***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wagner et al. (U.S. Patent No. 6,295,519) discloses a method and apparatus for coupling multiple computer peripherals to a computer system through a single I/O port. Cohen et al. (U.S. Patent No. 5,909,464) discloses a serial communications interface that supports multiple interface standards. Nagasawa et al. (U.S. Patent No. 6,965,950) discloses a signal input and output apparatus that discriminates between a plurality of different devices each issuing unique control signals substantially simultaneously through a single transmission path.

***Response to Arguments***

5. Applicant's arguments filed 4/24/2007 have been fully considered but they are not persuasive.

Regarding Claims 1, 15, and 18, Applicant argues that "Johnson teaches away from switching between standards depending on the signal being transmitted or received." The examiner respectfully disagrees. Contrary to Applicant's argument, Johnson does in fact teach this limitation. The communications processor 22 receives cable identification bits 27, and according to this identification electronically switches between the line drivers 33 and 35, see Column 4, lines 43-46 and lines 54-59, and also Column 5, lines 25-30. Further, in order to transmit a X.21 signal from communication processor 22 over cable 16, for example, line driver 35 must be used in order for proper data transmission (ie. "electronically change between the first and the second standard depending on the signal *being transmitted* or received", as claimed).

Applicant also argues that "[n]o suggestion or motivation to combine the references to achieve Applicants' invention is explicitly present in Johnson or APSA", and further "it appears that the Examiner is implying that the suggestion or motivation to combine the references is implicit in Johnson and APSA." However, as Applicant has pointed out, "in order to establish a prima facie case of obviousness, 'there must be some suggestion or motivation, either in the references themselves *or in the knowledge generally available to one of ordinary skill in the art*, to modify the reference or the combine the reference teachings.' MPEP § 2142." Therefore, since the examiner has provided a motivation that would be obvious to one of ordinary skill in the art (the

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speeds of the IEEE 1394-1995/1394a-2000 and IEEE 1394b-2002 standards being faster than those of the V.35 and X.21 standards), the combination is proper.

Finally, Applicant argues that "APSA and Johnson are non-analogous art and it would not be obvious to one of ordinary skill in the art to combine the interface system of Johnson, with standard-specific cables, with the IEEE 1394 standards in APSA." The examiner respectfully disagrees. Firstly, AAPA and Johnson are in fact both within the same field of endeavor (e.g. configuring a single port to be able to transmit and receive data of differing protocols). Further, in response to applicant's argument that Johnson is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, even assuming Johnson was not in the same field of endeavor, the Johnson disclosure is reasonably pertinent to the particular problem with which the Applicant was concerned (e.g. transmitting and receiving data of differing protocols at a single port).

Therefore, the claims stand as previously rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal Zaman whose telephone number is 571-272-6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm, alternate Fridays off.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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